

OptiMOS™³ Power-Transistor
Package

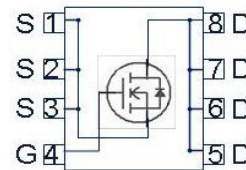
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications

Product Summary

V_{DS}	80	V
$R_{DS(on),max}$	12.3	m Ω
I_D	40	A



Type	BSZ123N08NS3 G
Package	PG-TSDSON-8
Marking	123N08N


Maximum ratings, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}, T_C=25^\circ\text{C}$	40	A
		$V_{GS}=10\text{ V}, T_C=100^\circ\text{C}$	35	
		$V_{GS}=10\text{ V}, T_A=25^\circ\text{C}, R_{thJA}=60\text{ K/W}^{2)}$	10	
Pulsed drain current ³⁾	$I_{D,pulse}$	$T_C=25^\circ\text{C}$	160	
Avalanche energy, single pulse	E_{AS}	$I_D=20\text{ A}, R_{GS}=25\ \Omega$	110	mJ
Gate source voltage	V_{GS}		± 20	V

¹⁾ J-STD20 and JESD22

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See figure 3 for more detailed information

⁴⁾ See figure 13 for more detailed information

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	66	W
		$T_A=25\text{ °C}$, $R_{\text{thJA}}=60\text{ K/W}^2$	2.1	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	-	1.9	K/W
Device on PCB	R_{thJA}	minimal footprint	-	-	62	K/W
		6 cm^2 cooling area ²⁾	-	-	60	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=33\text{ }\mu\text{A}$	2	2.8	3.5	
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}}=80\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{\text{DS}}=80\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=20\text{ A}$	-	10.3	12.3	m Ω
		$V_{\text{GS}}=6\text{ V}, I_{\text{D}}=10\text{ A}$	-	13.9	24	
Gate resistance	R_{G}		-	2	-	Ω
Transconductance	g_{fs}	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=20\text{ A}$	17	34	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	1300	1700	pF
Output capacitance	C_{oss}		-	350	470	
Reverse transfer capacitance	C_{rss}		-	15	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=1.6\ \Omega$	-	12	-	ns
Rise time	t_r		-	18	-	
Turn-off delay time	$t_{d(off)}$		-	19	-	
Fall time	t_f		-	4	-	

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	6.3	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	3.6	-	
Gate to drain charge	Q_{gd}		-	3.8	-	
Switching charge	Q_{sw}		-	6.5	-	
Gate charge total	Q_g		-	19	25	
Gate plateau voltage	$V_{plateau}$		-	4.9	-	V
Output charge	Q_{oss}	$V_{DD}=40\text{ V}, V_{GS}=0\text{ V}$	-	25	34	

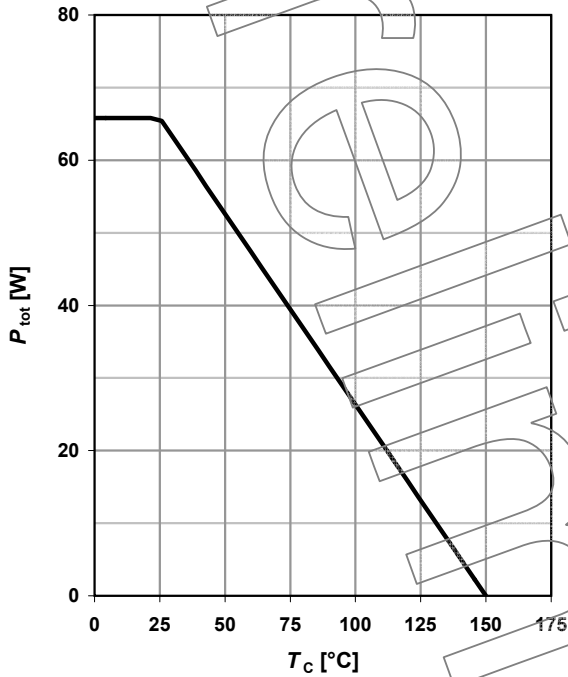
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	40	A
Diode pulse current	$I_{S,pulse}$		-	-	160	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=20\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.9	1.3	V
Reverse recovery time	t_{rr}	$V_R=40\text{ V}, I_F=20\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	45	-	ns
Reverse recovery charge	Q_{rr}		-	54	-	

⁵⁾ See figure 16 for gate charge parameter definition

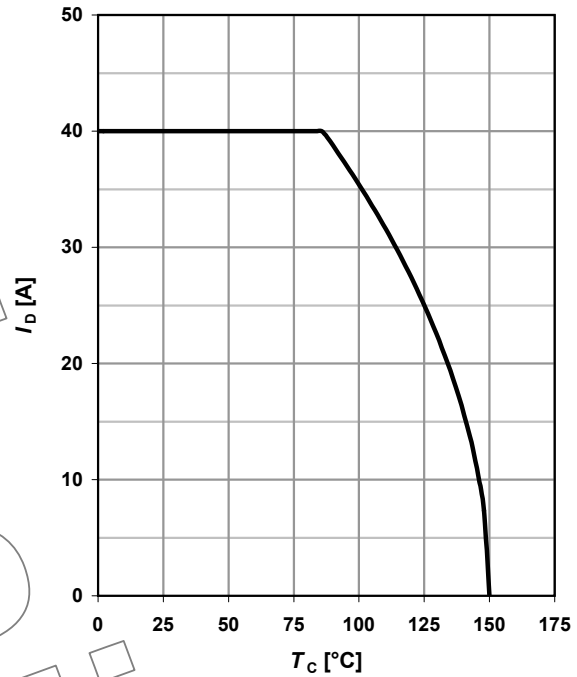
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

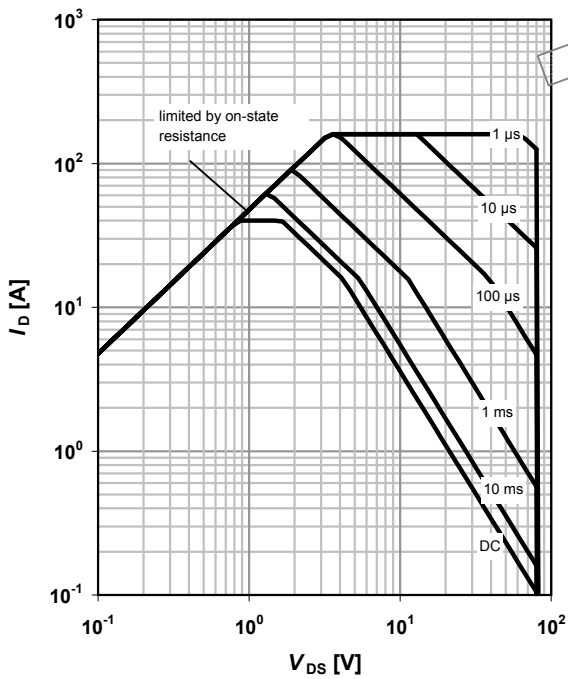
$I_D=f(T_C); V_{GS}\geq 10\text{ V}$



3 Safe operating area

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

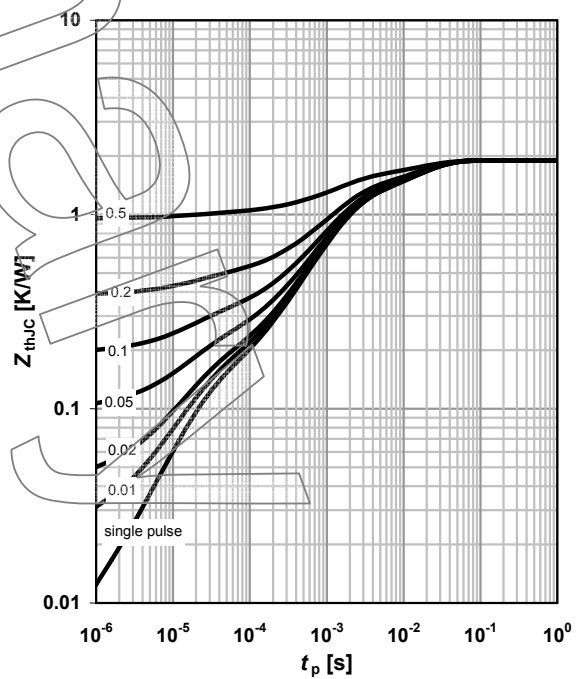
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

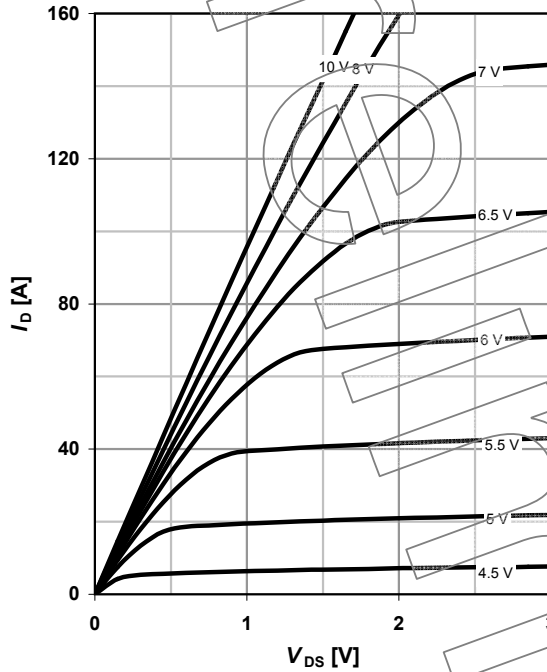
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

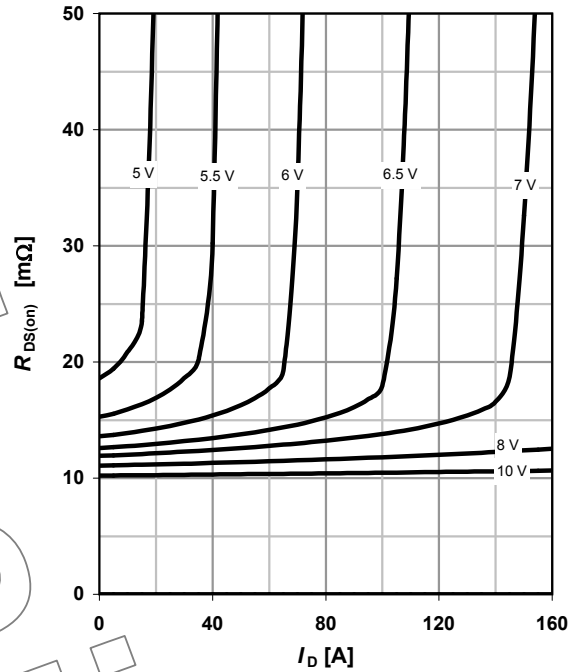
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

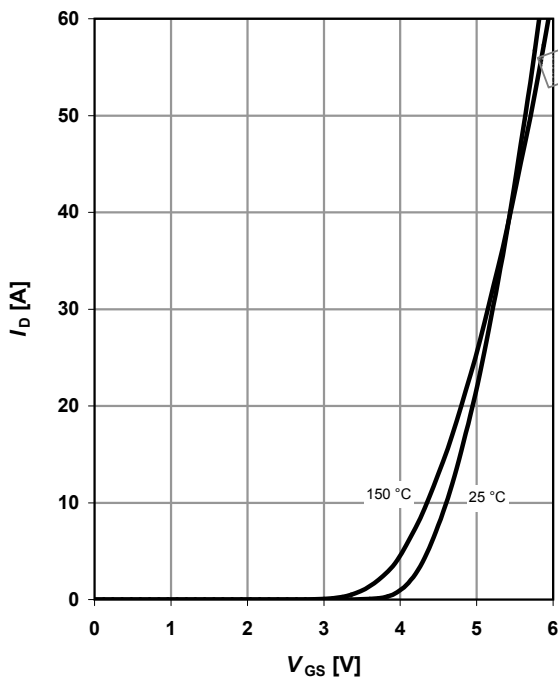
parameter: V_{GS}



7 Typ. transfer characteristics

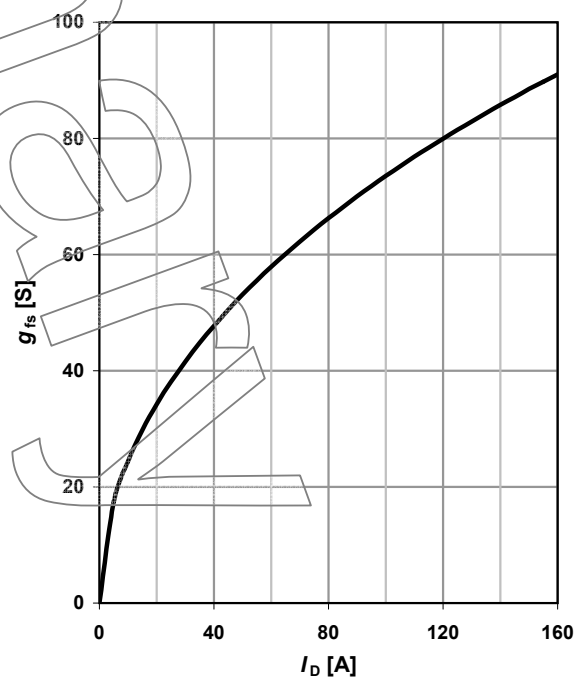
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



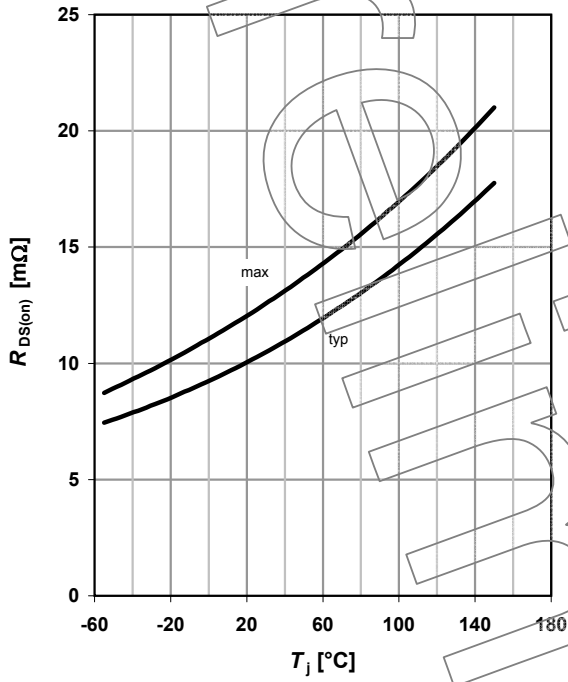
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



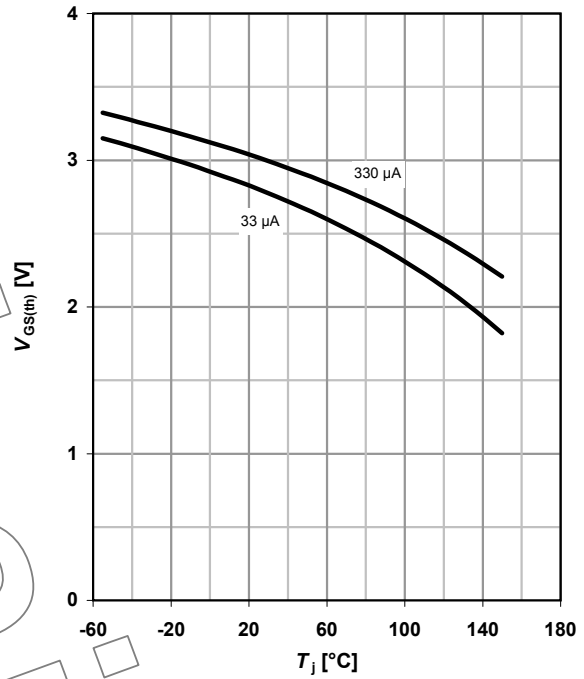
9 Drain-source on-state resistance

$R_{DS(on)} = f(T_j); I_D = 20 \text{ A}; V_{GS} = 10 \text{ V}$



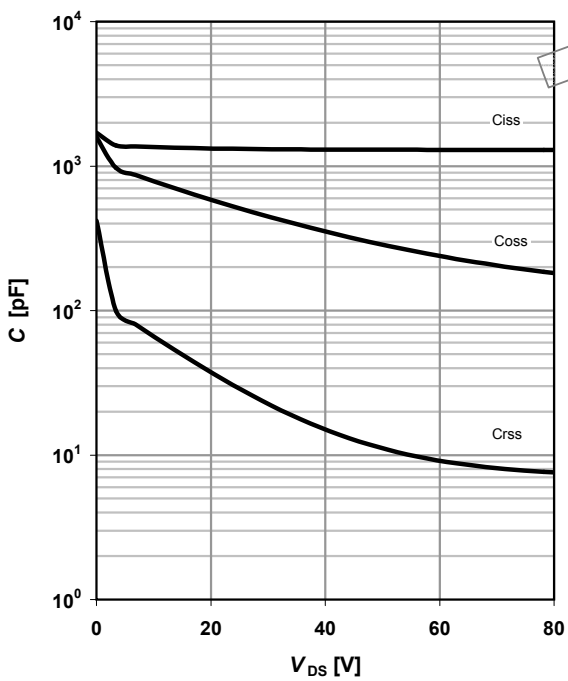
10 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$



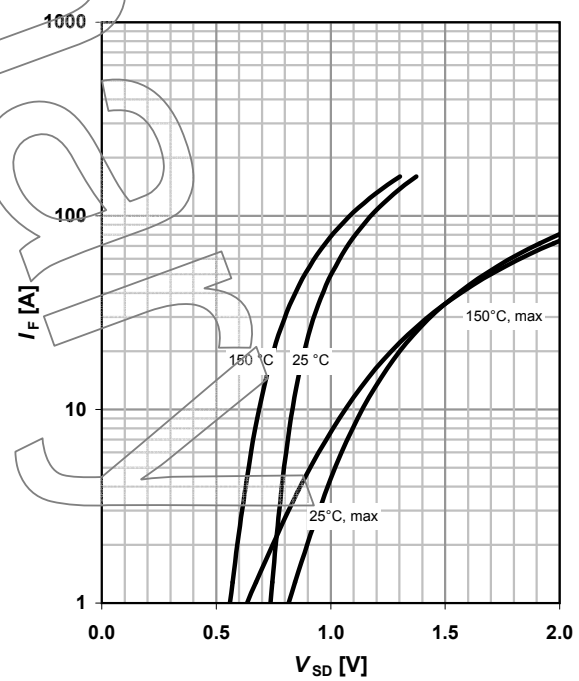
11 Typ. capacitances

$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



12 Forward characteristics of reverse diode

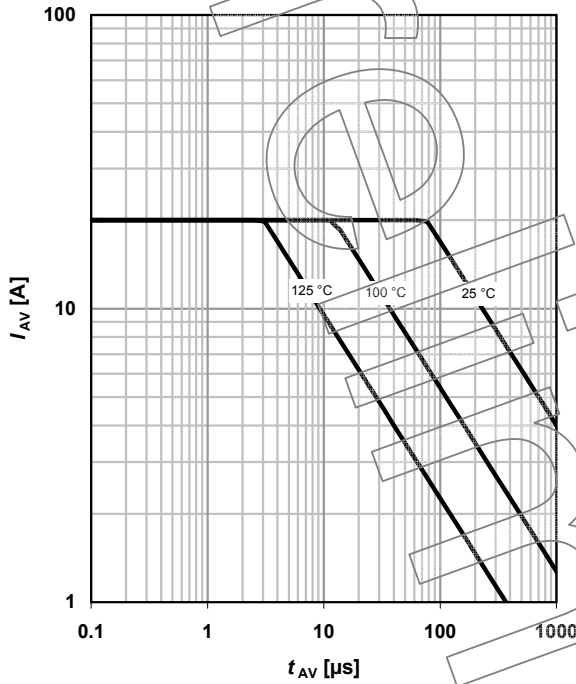
$I_F = f(V_{SD})$
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

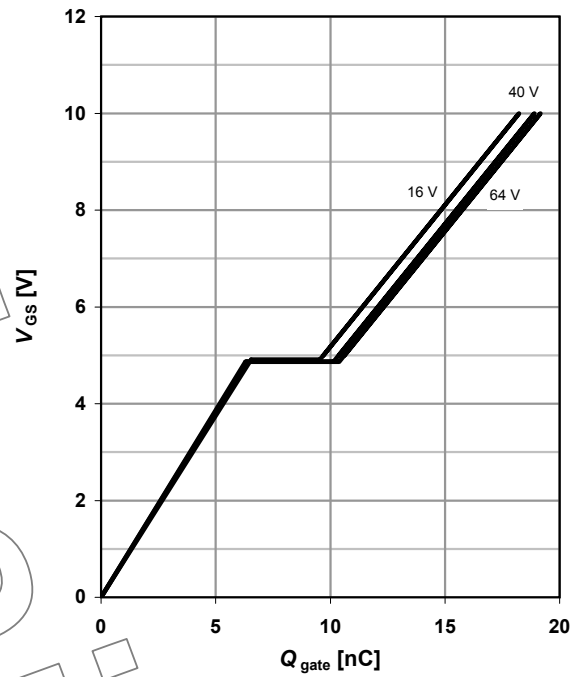
parameter: $T_{j(start)}$



14 Typ. gate charge

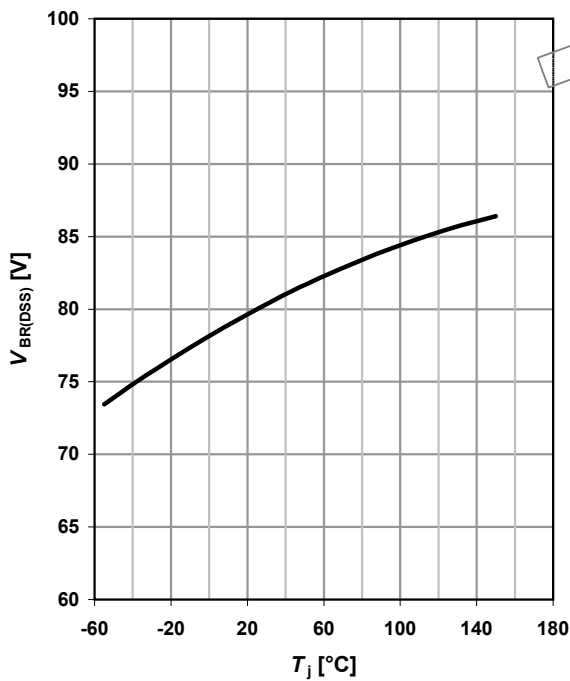
$V_{GS}=f(Q_{gate}); I_D=20 \text{ A pulsed}$

parameter: V_{DD}

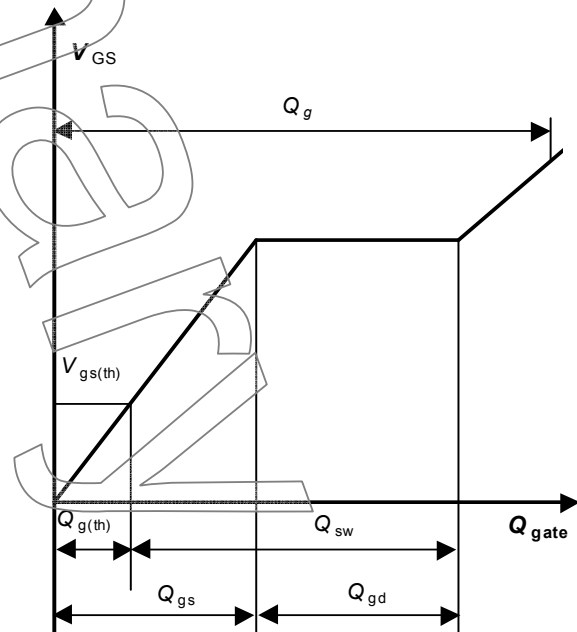


15 Drain-source breakdown voltage

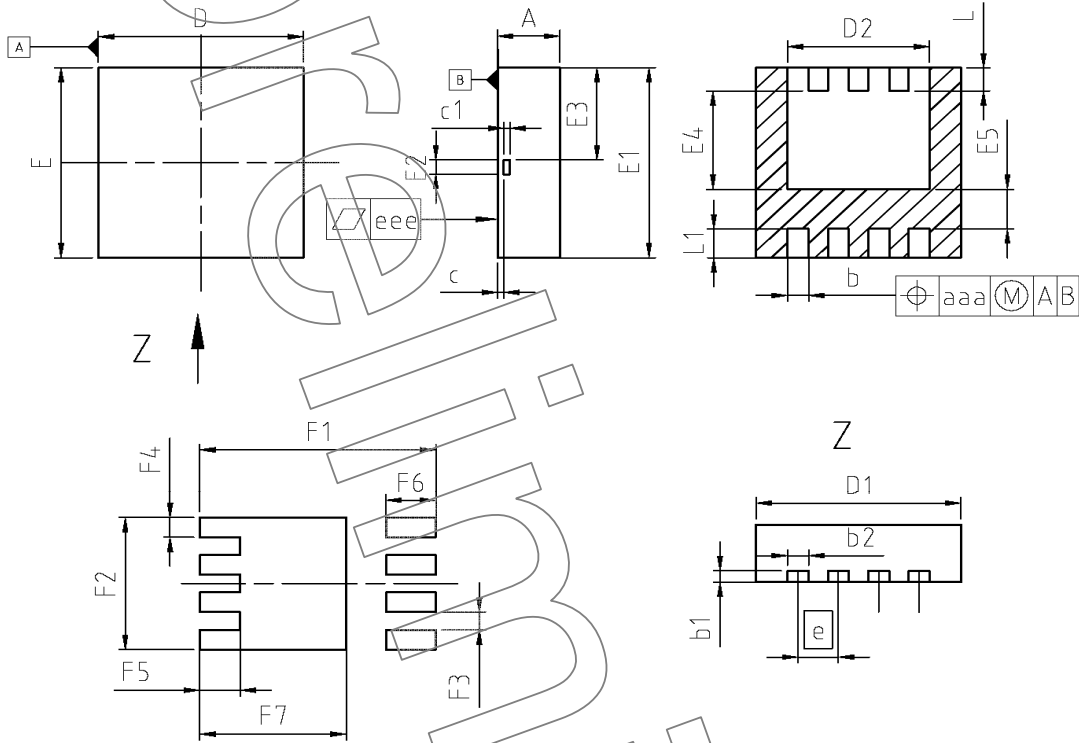
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



16 Gate charge waveforms



PG-TSDSON-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.95	1.00	0.037	0.039
b	0.25	0.35	0.010	0.014
b1	0.10	0.30	0.004	0.012
b2	0.20	0.40	0.008	0.016
c	0.00	0.20	0.000	0.008
D=D1	3.20	3.40	0.126	0.134
D2	2.15	2.35	0.085	0.093
E=E1	3.20	3.40	0.126	0.134
E2	0.10	0.30	0.004	0.012
E3	1.35	1.55	0.053	0.061
E4	1.60	1.80	0.063	0.071
E5	0.66	0.86	0.026	0.034
e	0.60	0.70	0.024	0.028
N	8		8	
L	0.31	0.51	0.012	0.020
L1	0.33	0.53	0.013	0.021
aaa	0.25		0.010	
eee	0.05		0.002	
F1	3.70	3.90	0.146	0.154
F2	2.19	2.39	0.086	0.094
F3	0.21	0.41	0.008	0.016
F4	0.24	0.44	0.009	0.017
F5	0.55	0.75	0.022	0.030
F6	0.70	0.90	0.028	0.035
F7	2.26	2.46	0.089	0.097

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